REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-18 are pending. Claims 1-18 stand rejected. Claims 19-32 are withdrawn.

Claims 1, 2, 7, 9, and 10 have been amended. Claims 5, 8, and 12 - 32 have been cancelled. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Rejections Under 35 U.S.C. § 112

The Examiner has rejected claims 2, 4-7, 12 and 17 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. The Examiner has stated that

> In claim 7 and 17, lines 3, using the term "...such as..." render scope of the claim being unclear whether the subsequent limitations are parts of the claims. The term "such as" should be deleted.
>
> Meaning and scope of "barrier/seed" as claims 2, 9, and 12 are unclear, since dependent claim 5 indicates "/" as --and--. It should be --barrier and seed--.
>
> (Dependent claim are rejected as depending on rejected base claim)

(p. 2, Office Action 9/17/03)

In response, applicants have amended claims 2, 7, and 9 to more distinctly claim the invention. Applicants have cancelled claims 5 and 17.

Rejections Under 35 U.S.C. 102(b)

Claim 1 stands rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,627,106 , of Hsu ("Hsu"). Claims 1, 3, 7 and 11 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Fan, et al. ("Fan"), Article of "Copper Wafer Bonding".

Applicants respectfully submit that claim 1, as amended, is not anticipated by Hsu or Fan under 35 U.S.C. 102§(b).

Claim 1, as amended, includes the following limitations.

A method of vertically stacking wafers, comprising:

> selectively depositing a plurality of metallic lines on opposing surfaces of each of a first wafer and a second wafer;
>
> bonding the first wafer to the second wafer by bonding the respective metallic lines on opposing surfaces of the first wafer and the second wafer to create a vertically stacked wafer pair,
>
> forming one or more vias to establish electrical connections between the active devices on each wafer of the vertically stacked wafer pair and an external interconnect, the vias tapered from top to bottom hole, such that a top surface of each via has a larger area than a bottom surface; and
>
> bonding two vertically stacked wafer pairs together by bonding the top surfaces of each of the one or more vias of a first vertically stacked wafer pair to corresponding top surfaces of each of the one or more vias of a second vertically stacked wafer pair.

(Claim 1)(Emphasis added)

Applicants respectfully submit that neither Hsu nor Fan teach or disclose the limitation of bonding two vertically stacked wafer pairs together by bonding top surfaces of tapered vias. Given that claims 3, 7, and 11 depend from claim 1, applicants respectfully submit that claims 3, 7, and 11 are, likewise, not anticipated by Hsu or Fan.

Rejections Under 35 U.S.C. § 103(a)

Claims 2, 4-6, 9-10, and 12-17 stand rejected under 35 U.S.C. § 103 as being unpatentable over Fan, et al. ("Fan"), Article of "Copper Wafer Bonding" taken with U.S. Patent No. 6,100,181 of You, et al. ("You") and McDonald ("McDonald"), Article of "Face to Face Wafer Bonding...".

It is respectfully submitted that Fan does not teach or suggest a combination with McDonald and that McDonald does not teach or suggest a combination with Fan. It would be impermissible hindsight based on applicants' own disclosure to incorporate the copper wafer bonding of Fan with McDonald. Moreover, such a combination would still lack the limitation of bonding two vertically stacked wafer pairs together by bonding top surfaces of tapered vias as discussed above in reference to claim 1. Given that claims 2-4, 6, 9 and 10 depend, directly or indirectly from claim 1, applicants respectfully submit that claims 2-4, 6, 9 and 10 are, likewise, not rendered obvious by the combination of Fan and McDonald.

Claims 8 and 18 stand rejected under 35 U.S.C. § 103 as being unpatentable over Fan, et al. ("Fan"), Article of "Copper Wafer Bonding" as applied to claims 1, 3, 7 and 11 above, and further in view of U.S. Patent No. 5,473,197 of Idaka, et al. ("Idaka") or U.S. Patent No. 5,455,445 of Kurtz ("Kurtz").

The Examiner has stated that

> Fan teaches a method as applied to base claims 1 and 12 above.
>
> Fan lacks forming the vias having tapered shape.
>
> However, Idaka teaches (at Figs. 8C-9C; col. 6, lines 33-67) forming the vias having tapered shape. Kurtz also teaches (at Fig. 1; col. 2) forming the vias 18a-d having a tapered shape from top to bottom of the via.

(Page 5, Office Action 9/17/03)

Idaka discloses

That is, as shown in FIG. 8A, groove portions 17 are formed in the photoresist film 15 only in positions between openings 16. When the photoresist film 15 is subjected to the heat treatment after the groove portions 17 are thus formed, the upper end portions of the openings 16 are significantly contracted in both of the directions towards the element regions 20 of the LSI chip 1 and towards the periphery thereof. Therefore, if the photoresist film 15 is removed after the inner wall of the opening 16 is plated with gold, bump electrodes 3 shown in FIGS. 8B, 8C can be formed. That is, the upper surface of the bump electrode 3 extends in two directions towards the element region 20 of the LSI chip 1 and the periphery of the LSI chip 1.

According to this embodiment, the bump electrode 3 in which the area of the bottom surface is the same as that of the first embodiment and the area of the bottom surface is larger than that of the first embodiment can be formed. Further, the upper surface of the bump electrode 3 does not extend in the arrangement direction of the bump electrodes 3. For this reason, even if the distance between the pads is reduced, the distance between the bump electrodes 3 can be made sufficiently long.

Next, a third embodiment of this invention is explained with reference to FIGS. 9A, 9B, 9C, 9D. In this embodiment, bump electrodes are formed by a transferring bump system. In FIGS. 9A, 9B, 9C, 9D, portions which are the same as those of FIGS. 1 to 4 are denoted by the same reference numerals.

First, as indicated by broken lines in FIG. 9A, a photoresist 32 having an opening 33 and a groove 34 is formed by the method explained with reference to FIGS. 3A and 3B, on the upper surface of the structure which is comprised of a glass substrate 31 and an ITO film (not shown) made of indium, tin and oxide formed on the substrate 31. Like the groove 17 described above, the groove 34 is formed along...

(Idaka, col. 6, lines 33-67) (Emphasis added)

Kurtz discloses

...material may be used and that the same may be doped n- or p-type as desired.

BRIEF DESCRIPTION OF THE DRAWINGS

The above-mentioned and other features and objects of the present invention and the manner of obtaining them will become apparent and the invention itself will be best understood by reference to the following description of an embodiment of the invention taken in conjunction with the accompanying drawings, wherein:

FIG. 1 is an exploded perspective view of an illustrative embodiment of a three dimensional integrated circuit structure fabricated in accordance with the present invention; and

FIGS. 2A-2G are a series of view depicting a method of fabricating one of a plurality of device wafers which, when bonded together, may be utilized to fabricate a three dimensional integrated circuit structure in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which an illustrative embodiment of the present invention is shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiment set forth herein. Rather, applications provide this embodiment so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art.

Referring to FIG. 1, a three dimensional integrated circuit chip structure 10 fabricated in accordance with the present invention is shown in exploded perspective view for ease of understanding. As seen in FIG. 1, the structure 10 comprises a plurality of individual integrated circuit device layers 12a-12e which are superposed and bonded together at layer bond interfaces 13a-13c to form a unitary structure. The bonding of the device layers can be accomplished by using glass bonding, electrostatic glass bonding; or any other well known technique. Fabricated on a surface of at least one of the device layers are one or more circuit devices as 14, 15, and 16 of upper layer 12a. As can be seen in FIG. 1, each device layer further comprises one or more electrical contacts as 18a-18d of layer 12b, which contacts extend through the thickness thereof to form an electrically conductive path therethrough. The respective contacts of intermediate device layer 12b are bonded to corresponding aligned contacts of an overlying or underlying device layer. Cavities 50a-50c receive the one or more circuit devices of an underlying device layer. Thus, as will be readily ascertained by those skilled in the art that any desired number of device layers may be interconnected in this manner to provide a densely arranged, three dimensional structure having conductive pathways extending therethrough.

As will be appreciated by those skilled in the art, various combinations of devices may be incorporated in the device layers. In the illustrative embodiment of FIG. 1, the bottom device layer 12e is configured as a pressure sensor device having a diaphragm 20 and having sensor elements 24 and 28 fabricated thereon. Any conventional technique for fabricating such a sensor device layer may be utilized. Reference may be had, for example, to U.S. patent application Ser. No. 08/058,016 entitled SEMICONDUCTOR ISOLATED STRUCTURES HAVING ENVIRONMENTALLY ISOLATED ELEMENTS AND METHOD FOR MAKING THE...

(Kurtz, col. 2) (Emphasis added)

Applicants respectfully submit that amended claim 1 is not rendered obvious by Fan in combination with either Idaka or Kurtz.

It is respectfully submitted that Fan does not teach or suggest a combination with Idaka and that Idaka does not teach or suggest a combination with Fan. It would be impermissible hindsight based on applicants' own disclosure to incorporate the copper wafer bonding of Fan with the trapezoidal bump electrode device of Idaka. Vias extend through the dielectric whereas bump electrodes extend from and above the substrate. Moreover, such a combination, as well as the combination of Fan and Kurtz, would still lack the limitation of bonding two vertically stacked wafer pairs together by bonding top surfaces of tapered vias, as discussed above in reference to claim 1.

None of Fan, Idaka, or Kurtz, alone, or in combination, teach bonding the larger surface areas of tapered vias. Fan does not teach tapered vias and Idaka teaches tapered bump electrodes not vias, as noted above. If the bump electrodes were bonded, one to another, it would weaken, not strengthen, the bond between the wafers of Fan. Kurtz does not mention that the electrical contacts are tapered. Kurtz, at Figure 1, shows what appear to be tapered electrical contacts, but Kurts shows the electrical contacts bonded one to another from top to bottom (not top to top). This is because the device layers of Kurtz are bonded, one to another, using "glass bonding, electrostatic glass bonding, or any other well-known technique." Therefore, Kurtz not only shows the electrical contacts bonded from top to bottom, but teaches away from using such a bond mechanically.

For these reasons, applicants respectfully submit that amended claim 1 is not rendered obvious by the combination of Fan with either Idaka or Kurtz. Given that claims 2 – 11 depend, directly or indirectly, from claim 1, applicants respectfully submit that claims 2 – 11 are, likewise, not rendered obvious by the combination of Fan with either Idaka or Kurtz.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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